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EXAMINER	
VIEAUX, GARY	
ART UNIT	**PAPER NUMBER**
2612	5

DATE MAILED: 07/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/779,528	SUZUKI ET AL.	
	Examiner	Art Unit	
	Gary C. Vieaux	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

2. Claims 2, 3, 13 and 14 are objected to because of the following informalities: claim 2 recites "said output signal line" in line 2, and claim 3 recites "said output signal line" in line 2 - there is insufficient antecedent basis for this limitation in the claim (claim 1 recites "at least one output signal line"); also, "converter" is misspelled in line 3 of claim 13, and again in line 2 of claim 14. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The language "in a space as viewed in plan between the pair" is not clearly understood. This claim will be directly addressed on its merits as best interpreted/understood by the examiner.

Claim Rejections - 35 USC § 103

5. **Claims 1- 5, 13, and 15-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Lee et al. (EU 0 932 302 A2), and in further view of Watanabe (US #6,522,365.)

6. Regarding claim 1, the applicants, in their Description of the Related Art, disclose the prior art teaching of a solid-state image pickup device comprising: a number of photoelectric conversion elements disposed in a matrix layout in the principal surface of a semiconductor (p. 1 line 24 – p.2 line 1); a switching circuit unit provided per each photoelectric conversion element, said switching circuit unit including an output transistor capable of generating an electric signal representing an amount of a signal charge accumulated in a corresponding photoelectric conversion element (p. 2 lines 1-7); a row select signal wiring line provided per each photoelectric conversion element row and extending along a corresponding photoelectric conversion element row, said row select signal wiring line supplying a row select signal to each corresponding switching circuit units, the row select signal controlling generation of the electric signal (p. 2 lines 15-21); an analog/digital conversion unit provided for each photoelectric conversion element column (p. 2 lines 3-4); and at least one output signal line provided per each analog/digital conversion unit, the output signal line electrically connecting said analog/digital conversion unit and the output transistor provided for each photoelectric conversion element in at least one of the photoelectric conversion element columns corresponding to said analog/digital conversion unit (p. 2 lines 2-12.) The admitted prior art, however, discloses neither a teaching of an analog/digital conversion unit provided

for each pair of adjacent photoelectric conversion element columns, nor a teaching of a number of photoelectric conversion elements disposed in a plurality of rows and columns in a surface of a semiconductor substrate, each photoelectric conversion element of a photoelectric conversion element column of an even number being shifted in a column direction by about a half pitch between photoelectric conversion elements in each photoelectric conversion element column, relative to each photoelectric conversion element of a photoelectric conversion element column of an odd number, and each photoelectric conversion element of a photoelectric conversion element row of an even number being shifted in a row direction by about a half pitch between photoelectric conversion elements in each photoelectric conversion element row, relative to each photoelectric conversion element of a photoelectric conversion element row of an odd number, so that each photoelectric conversion element row includes photoelectric conversion elements of only in the odd or even columns.

7. Nevertheless, Lee not only teaches a solid-state image pickup device comprising a number of photoelectric conversion elements disposed in a plurality of rows and columns in a surface of a semiconductor substrate (col.2 lines 25-28), but also teaches analog/digital conversion on a per-n-column basis (col. 5, lines 35-37; col. 6 lines 46-47.) A per-n-column conversion basis implies more than one column being processed by a single converter, with a conversion of two adjacent columns understandably fitting within that basis. It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ analog/digital conversion on pairs of adjacent columns as taught by Lee, with the image pickup device of admitted prior art. One of

ordinary skill in the art at the time the invention was made would be motivated to employ this parallel-column pixel readout to reduce the conversion speed of the analog/digital converter to the line scan time (col. 6, lines 52-55.)

8. Furthermore, Watanabe teaches a number of photoelectric conversion elements disposed in a plurality of rows and columns, each photoelectric conversion element of a photoelectric conversion element column of an even number being shifted in a column direction by about a half pitch between photoelectric conversion elements in each photoelectric conversion element column, relative to each photoelectric conversion element of a photoelectric conversion element column of an odd number, and each photoelectric conversion element of a photoelectric conversion element row of an even number being shifted in a row direction by about a half pitch between photoelectric conversion elements in each photoelectric conversion element row, relative to each photoelectric conversion element of a photoelectric conversion element row of an odd number, so that each photoelectric conversion element row includes photoelectric conversion elements of only in the odd or even columns (Fig. 1 C.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the pixels in a manner similar to that taught by Watanabe, with the with the image pickup device of admitted prior art and Lee. One of ordinary skill in the art at the time the invention was made would have been motivated to create this arrangement to obtain high spatial resolution (col. 4 lines 50-54.)

9. Regarding claim 2, the admitted prior art, Lee, and Watanabe teach all of the limitations of claim 2 (see the 103(a) rejection to claim 1 supra), including a teaching

wherein an output signal line is provided for each photoelectric conversion element column and extends along a corresponding photoelectric conversion element column; and said analog/digital conversion unit is provided for two output signal lines. The admitted prior art teaches an output signal line connecting each photoelectric conversion unit, via the switching circuit units, to the analog/digital conversion unit for each photoelectric conversion element column (p. 2 lines 1-4) as well as one output signal line per each photoelectric conversion element column (p. 4 lines 1-2.) Lee teaches a similar configuration with the addition of output signals from multiple columns being converted by one analog/digital conversion unit (Fig. 4; col.6 lines 41-47.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide one analog/digital conversion unit for two output signals as taught by Lee, with the image pickup device and output signal line arrangement as taught by the admitted prior art, Lee, and Watanabe. One of ordinary skill in the art at the time the invention was made would be motivated to provide one analog/digital conversion unit for two output signal lines so that pixel readout was column-parallel, reducing the conversion speed of the analog/digital conversion unit to the line scan time (col. 6 lines 51-55.)

10. Regarding claim 3, the admitted prior art, Lee and Watanabe teach all of the limitations of claim 3 (see the 103(a) rejection to claim 1 supra), including a teaching wherein an output signal line is provided for each said pair of adjacent photoelectric conversion element columns; and said analog/digital conversion unit is provided per each output signal line. The admitted prior art provides a teaching wherein an output

signal line is provided per each photoelectric conversion element column and an analog/digital conversion unit is provided per each output signal line (p. 4 lines 1-3.) Additionally, Lee provides a teaching wherein said output signal line (via the CDS) is provided for each said pair (per-n-column) of adjacent photoelectric conversion element columns in a space between the pair (Fig. 4.) It is noted that since an analog/digital converter operates on one inputted value at a time when converting, the outputted signal values of per-n-columns, with per-n-output signal lines, must eventually channel into the analog/digital converter by means of a single line. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide one output signal line, originating from more than one column, for the analog/digital conversion unit as taught by Lee, with the image pickup device and output signal line arrangement as taught by the admitted prior art, Lee, and Watanabe. One of ordinary skill in the art at the time the invention was made would be motivated to employ this circuitry design so that eventually only one line was fed into the analog/digital converter for conversion of a particular signal.

11. Regarding claim 4, the admitted prior art, Lee, and Watanabe teach all of the limitations of claim 4 (see the 103(a) rejection to claim 1 supra), including a teaching by the admitted prior art wherein the solid-state image pickup device further comprises a first scan unit for supplying the row select signal to each row select signal wiring line at a predetermined timing (p. 2 lines 22-24.) It is noted that Lee also teaches a scan unit for supplying the row select signal (col. 6 lines 19-28.)

12. Regarding claim 5, the admitted prior art, Lee, and Watanabe teach all of the limitations of claim 5 (see the 103(a) rejection to claim 4 supra), including a teaching by the admitted prior art wherein the solid-state image pickup device further comprises a control unit for controlling an operation of said first scan unit, in addition to the operation of the analog/digital units, the buffer memory, and the like (p. 3 lines 7-8.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to understand that a control unit which controls the operation of multiple units as taught by the admitted prior art, may be substituted by several separate control units, each controlling an operation of a separate unit, for example, employing a separate control unit for controlling an operation of a first scan unit for supplying the row select signal.

13. Regarding claim 13, admitted prior art, Lee, and Watanabe teach all of the limitations of claim 13 (see the 103(a) rejection to claim 1 supra), including a teaching by the admitted prior art wherein each of said analog/digital conversion units includes a sample/hold circuit unit having a capacitor (p. 4 line 3), and an analog/digital converter for converting an output of said sample/hold circuit unit into a digital signal (p. 1 lines 21-23.)

14. Regarding claim 15, the admitted prior art, Lee, and Watanabe teach all of the limitations of claim 15 (see the 103(a) rejection to claim 1 supra), as well as a teaching by the admitted prior art wherein the solid-state image pickup device further comprises a control unit for controlling an operation of each of said analog/digital conversion units, in addition to the operation of the scan unit to supply the row select signal, the buffer memory and the like (p. 3 lines 7-8.) It would have been obvious to one of ordinary skill

in the art at the time the invention was made to understand that a control unit which controls the operation of multiple units as taught by the admitted prior art, may be substituted by several separate control units, each controlling an operation of a separate unit, for example, employing a separate control unit for controlling an operation of each of the analog/digital conversion units.

15. Regarding claim 16, the admitted prior art, Lee, and Watanabe teach all of the limitations of claim 16 (see the 103(a) rejection to claim 1 supra), including a teaching by the admitted prior art wherein the solid-state image pickup device further comprises a buffer memory unit for temporarily storing the digital signals output from each of said analog/digital conversion units (p.2 lines 13-14) and a teaching by Lee wherein the buffer memory outputs the digital signals (EP '302 col. 5, lines 26-32.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to output the digital signal after buffering as taught by Lee, with the buffer memory unit of the solid state image pickup device as taught in the admitted prior art, Lee, and Watanabe. One of ordinary skill in the art at the time the invention was made would be motivated to buffer the digital signals prior to output to assist in controlling the flow of data when it is being provided to an image display or for motion capture by frame storage (EP '302 col. 5, lines 26-32.)

16. Regarding claim 17, the admitted prior art, Lee, and Watanabe teach all of the limitations of claim 17 (see the 103(a) rejection to claim 1 supra), as well as a teaching by the admitted prior art wherein the solid-state image pickup device further comprises a control unit for controlling an operation of said buffer memory unit, in addition to the

operation of the scan unit to supply the row select signal, analog/digital conversion units, and the like (p. 3 lines 7-8.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to understand that a control unit which controls the operation of multiple units as taught by the admitted prior art, may be substituted by several separate control units, each controlling an operation of a separate unit, for example, employing a separate control unit for controlling an operation of said buffer memory unit.

17. **Claims 6-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, Lee, and Watanabe as applied to claim 1 above, and further in view of Gowda et al. (US #5,898,168.)

18. Regarding claim 6, the admitted prior art, Lee, and Watanabe teach all of the limitations of claim 6 (see the 103(a) rejection to claim 1 supra), except for a teaching wherein the device is further comprising at least one power supply voltage wiring line electrically connected to each of said output transistors for supplying a power supply voltage to the output transistors, wherein: each of said output transistors receives at its control terminal the electric signal representing the amount of the signal charge accumulated in a corresponding photoelectric conversion element; and each of said switching circuit units further comprises a row select transistor connected to said output transistor by serial connection, said row select transistor receiving at its control terminal the row select signal, the serial connection being interposed between a corresponding output signal line and said power supply voltage wiring line with electrically connecting

to the output signal line and power supply voltage wiring line. However, the admitted prior art does teach the output transistor generating an electric signal representing an amount of a signal charge accumulated in a corresponding photoelectric conversion element (p. 2, lines 4-7.) Gowda teaches a device which has at least one power supply voltage wiring line (Fig 1, indicator VDD; Fig. 2 indicator 19) electrically connected to each of said output transistors for supplying a power supply voltage to the output transistors (Fig 1, indicator 11), wherein: each of said output transistors receives at its control terminal the electric signal representing the amount of the signal charge accumulated in a corresponding photoelectric conversion element (Fig 1 indicator 17; prior art p. 2, lines 4-7); and each of said switching circuit units further comprises a row select transistor (Fig 1, indicator 12) connected to said output transistor by serial connection, said row select transistor receiving at its control terminal the row select signal (Fig. 1 VROW; col. 1 lines 44-46), the serial connection being interposed between a corresponding output signal line and said power supply voltage wiring line with electrically connecting to the output signal line and power supply voltage wiring line (Fig 1.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the circuitry as taught by Gowda, with the image pickup device as taught by the admitted prior art, Lee, and Watanabe. One of ordinary skill in the art at the time the invention was made would be motivated to use this circuitry when creating a CMOS based image sensor with signal processing circuits that can be readily integrated on the same chip as the image sensor, thus enabling the design of smart,

single-chip camera systems, in addition to creating a financial savings due to associated manufacturing costs (col. 1 lines 18-27.)

19. Regarding claim 7, the admitted prior art, Lee, Watanabe, and Gowda teach all of the limitations of claim 7 (see the 103(a) rejection to claim 6 supra), including a teaching by Gowda wherein each of said switching circuit units further comprises a reset transistor (Fig 1 indicator 11) electrically connected to a corresponding photoelectric conversion element (Fig. 1 indicator 6) and said power supply voltage wiring line (Fig 1 indicator VDD; Fig. 2 indicator 19), said reset transistor being interposed between a control terminal of said corresponding output transistor (Fig. 1 indicator 13) and said power supply voltage wiring line (Fig 1 indicator VDD); and the solid-state image pickup device further comprises a reset signal supply wiring line provided for each photoelectric conversion element row and extending along a corresponding photoelectric conversion element row, said reset signal supply wiring line being electrically connected to control terminals of corresponding reset transistors (Fig. 1 and Fig. 2 indicator RES; col. 1 lines 46-48.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the circuitry as taught by Gowda, with the image pickup device as taught by the admitted prior art, Lee, and Watanabe. One of ordinary skill in the art at the time the invention was made would be motivated to use this circuitry when creating a CMOS based image sensor with signal processing circuits that can be readily integrated on the same chip as the image sensor, thus enabling the design of smart, single-chip camera systems, in addition to creating a financial savings due to associated manufacturing costs (col. 1 lines 18-27.)

20. Regarding claim 8, the admitted prior art, Lee, Watanabe, and Gowda teach all of the limitations of claim 8 (see the 103(a) rejection to claim 7 supra), including a teaching by Lee of a controller for generating reset signals (Fig. 4 indicator 114; col. 6 lines 19-28.) It is also noted that Gowda provides a teaching wherein the device has a unit (Fig. 2 indicator 14) for supplying a control signal for said reset transistor to each of said reset signal supply wiring lines at a predetermined timing (Fig. 1 and 2, indicator RES; col. 1 lines 46-48 and 61-62.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a unit as taught by Lee, with the image pickup device as taught by the admitted prior art, Lee, Watanabe, and Gowda. One of ordinary skill in the art at the time the invention was made would be motivated to incorporate this unit into the device in order to supply control signals for control of the reset transistors. Additionally, Lee teaches a unit that supplies not only reset signals, but also select and transfer signals (Fig. Indicator 114; col. 6 lines 25-28.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to understand that a unit which supplies multiple control signals as taught Lee, may be substituted by several separate units, each supplying a separate control signal, for example, employing a separate unit for supplying control signals for the reset transistors.

21. Regarding claim 9, the admitted prior art, Lee, and Watanabe teach all of the limitations of claim 9 (see the 103(a) rejection to claim 8 supra), as well as a teaching by the admitted prior art wherein the solid-state image pickup device further comprises a control unit for controlling an operation of a scan unit to supply the row select signal,

analog/digital conversion units, the buffer memory unit, and the like (p. 3 lines 7-8.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to understand that a control unit which controls the operation of multiple units as taught by the admitted prior art, may be substituted by several separate control units, each controlling an operation of a separate unit, for example, employing a separate control unit for controlling an operation of a second scan to supply the reset signal.

22. Regarding claim 10, the admitted prior art, Lee, and Watanabe teach all of the limitations of claim 10 (see the 103(a) rejection to claim 1 supra), except for a teaching wherein: each of said switching circuit units further comprises a transfer transistor electrically connected to a corresponding photoelectric conversion element and a corresponding output transistor, said transfer transistor being interposed between said corresponding photoelectric conversion element and said corresponding output transistor; and the solid-state image pickup device further comprises a transfer control signal supply wiring line provided for each photoelectric conversion element row and extending along a corresponding photoelectric conversion element row, said transfer control signal supply wiring line being electrically connected to control terminals of corresponding transfer transistors. Gowda teaches a device which has a transfer transistor electrically connected to a corresponding photoelectric conversion element and a corresponding output transistor (Fig. 1, indicator 8; col. 1 line 66), said transfer transistor (Fig. 1, indicator 8) being interposed between said corresponding photoelectric conversion element (Fig. 1, indicator 6) and said corresponding output

transistor (Fig. 1, indicator 13); and the solid-state image pickup device further comprises a transfer control signal supply wiring line provided for each photoelectric conversion element row and extending along a corresponding photoelectric conversion element row (Fig. 2 indicator 19), said transfer control signal supply wiring line being electrically connected to control terminals of corresponding transfer transistors (Fig. 1 indicators VTX and 8; col. 1 lines 57-59.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the circuitry as taught by Gowda, with the image pickup device as taught by the admitted prior art, Lee, and Watanabe. One of ordinary skill in the art at the time the invention was made would be motivated to use this circuitry when creating a CMOS based image sensor with signal processing circuits that can be readily integrated on the same chip as the image sensor, thus enabling the design of smart, single-chip camera systems, in addition to creating a financial savings due to associated manufacturing costs (col. 1 lines 18-27.)

23. Regarding claim 11, the admitted prior art, Lee, Watanabe, and Gowda teach all of the limitations of claim 11(see the 103(a) rejection to claim 10 supra), including a teaching by Gowda wherein the device has a scan unit (Fig. 2 indicator 14) for supplying a control signal for said transfer transistor (Fig. 1 indicator 8) to each of said transfer control signal wiring lines at a predetermined timing (Fig. 1 and 2, indicators VTX and 19; col. 1 lines 57-62.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a scan unit as taught by Gowda, with the image pickup device as taught by the admitted prior art, Lee, Watanabe, and Gowda. One of ordinary skill in the art at the time the invention was

made would be motivated to incorporate a scan unit into the device in order to supply control signals for control of the transfer transistors. Additionally, Lee teaches a unit that supplies not only transfer signals, but also reset and transfer signals (Fig. Indicator 114; col. 6 lines 25-28.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to understand that a unit which supplies multiple control signals as taught Lee, may be substituted by several separate units, each supplying a separate control signal, for example, employing a separate unit for supplying control signals for the transfer transistors.

24. Regarding claim 12, the admitted prior art, Lee, and Watanabe teach all of the limitations of claim 12 (see the 103(a) rejection to claim 11 supra), as well as a teaching by the admitted prior art wherein the solid-state image pickup device further comprises a control unit for controlling an operation of a scan unit to supply the row select signal, analog/digital conversion units, the buffer memory unit, and the like (p. 3 lines 7-8.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to understand that a control unit which controls the operation of multiple units as taught by the admitted prior art, may be substituted by several separate control units, each controlling an operation of a separate unit, for example, employing a separate control unit for controlling an operation of a third scan unit for supplying control signals for the reset transistors.

25. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, Lee, and Watanabe as applied to claim 13 above, in view of Gowda et al. (US #6,344,877.)

26. The admitted prior art, Lee, and Watanabe teach all of the limitations of claim 13 (see the 103(a) rejection to claim 13 supra), except for an explicit teaching wherein each of said analog/digital converter includes: a comparator for comparing a voltage of output signal output from said sample/hold circuit unit with a reference voltage signal, said comparator outputting a control operation signal when the reference voltage signal externally supplied to said comparator becomes equal to the voltage of output signal output from said sample/hold circuit; and a latch circuit for receiving the control operation signal and a count signal, latching the count of the count signal externally supplied to said latch circuit when the control operation signal is supplied, and outputting an electric signal represent the count latched. However, the admitted prior art does teach an A/D conversion unit having an analog/digital converter connected to the output of the sample/hold circuit unit (p. 1 lines 21-23), as well as the output signal line inputting a voltage to the analog/digital conversion unit, which in turn outputs a digital signal representing the analog voltage signal (p. 2 lines 9-14.) Gowda '877 teaches an analog/digital converter circuitry including: a comparator (Fig. 2 indicator 40) for comparing a voltage of output signal output (Fig. 2 indicator VOUT) with a reference voltage signal (Fig. 2 indicator VREF), said comparator outputting a control operation signal when the reference voltage signal externally supplied to said comparator becomes equal (col. 4 lines 53-55) to the voltage of output signal output (Fig. 2); and a

latch circuit (Fig. 2 indicator 42) for receiving the control operation signal and a count signal (Fig. 2 indicator D1), latching the count of the count signal externally supplied to said latch circuit when the control operation signal is supplied, and outputting an electric signal represent the count latched (col. 4 lines 55-61.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the analog/digital converter as taught by Gowda '877, to serve as the analog/digital converter receiving the output signal passed through the sample/hold unit of the image pickup device as taught by the admitted prior art, Lee, and Watanabe. One of ordinary skill in the art at the time the invention was made would be motivated to employ this circuitry design to perform correlated double sampling (CDS) in an attempt to remove noise associated with a reset switch, as well as provide room for other electronics and/or reduce the overall chip size (col. 2 lines 17-31; col. 3 lines 21-23; col. 4 lines 9-26.)

27. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Watanabe as applied to claim 1 above, and further in view of Park et al. (US #5,693,967.)

28. The admitted prior art, Lee, and Watanabe teach all of the limitations of claim 18 (see the 103(a) rejection to claim 1 supra), except for a teaching wherein the device further comprises a color filter disposed for each of said photoelectric conversion elements thereover; and a micro lens disposed for each of said color filters thereover. Park teaches a device with color filters disposed for each of said photoelectric

conversion elements thereover (Fig. 1B, indicator 24); and a micro lens disposed for each of said color filters thereover (Fig. 1B indicator 26.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to include color filters and micro lenses as taught by Park, with the image pickup device as taught by the admitted prior art, Lee, and Watanabe. One of ordinary skill in the art at the time the invention was made would be motivated to add color filters to selectively pass spectral components of a specific wavelength onto the photoelectric conversion element, and to further add micro lens to collect light onto the photoelectric conversion elements.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Decker et al., entitled "A 256 x 256 CMOS Imaging Array with Wide Dynamic Range Pixels and Column-Parallel Digital Output" (IEEE Journal of Solid-State Circuits, Vol. 33, no. 12) teaches two columns per analog/digital converter.

Mendis et al., entitled "A 128 x 128 CMOS Active Pixel Image Sensor for Highly Integrated Imaging Systems" (Electron Devices Meeting, 1993) teaches transistor configurations similar to the instant application.

Ackland et al. (US #5,541,402) teaches transistor configurations similar to the instant application.

Fossum et al. (US #5,471,515) teaches transistor configurations similar to the instant application.

Chi et al. (US #5,587,596) teaches transistor configurations similar to the instant application.

Dickenson et al. (US #5,602,585) teaches transistor configurations similar to the instant application.

Ishida et al. (US #6,046,466) teaches the use of micro lenses and color filters.

Aoki et al. (US #5,479,049) teaches the use of micro lenses and color filters.

Mehra et al. (US #5,118,924) teaches the use of micro lenses and color filters.

Yamada (US #6,236,434) teaches the use of micro lenses and color filters, as well as a pixel layout similar to the instant application.

Sekine (US #5,793,071 and US #4,602,289) teaches a pixel layout similar to the instant application.

Pain et al. (US #5,886,659) teaches the use of an A/D converter with more than 1 column.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary C. Vieaux whose telephone number is 703-305-9573. The examiner can normally be reached on Monday - Friday, 8:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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